Accurate Characterization of the Variability in Power Consumption in Modern Mobile Processors

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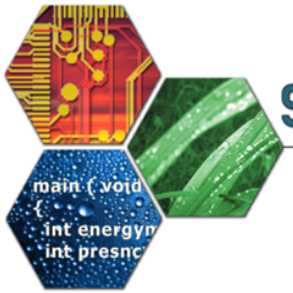
http://variability.org



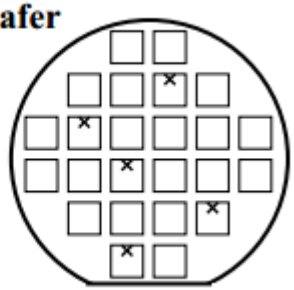
synergy

systems, networking and energy efficiency

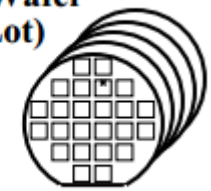
Variability Primer

Lot–to–Lot

Within Wafer



Wafer–to–Wafer
(or within Lot)



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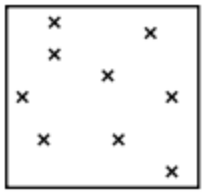
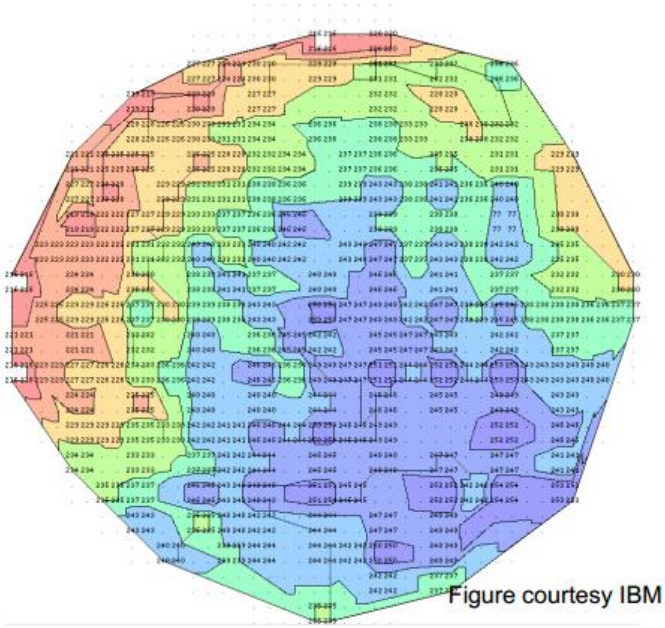


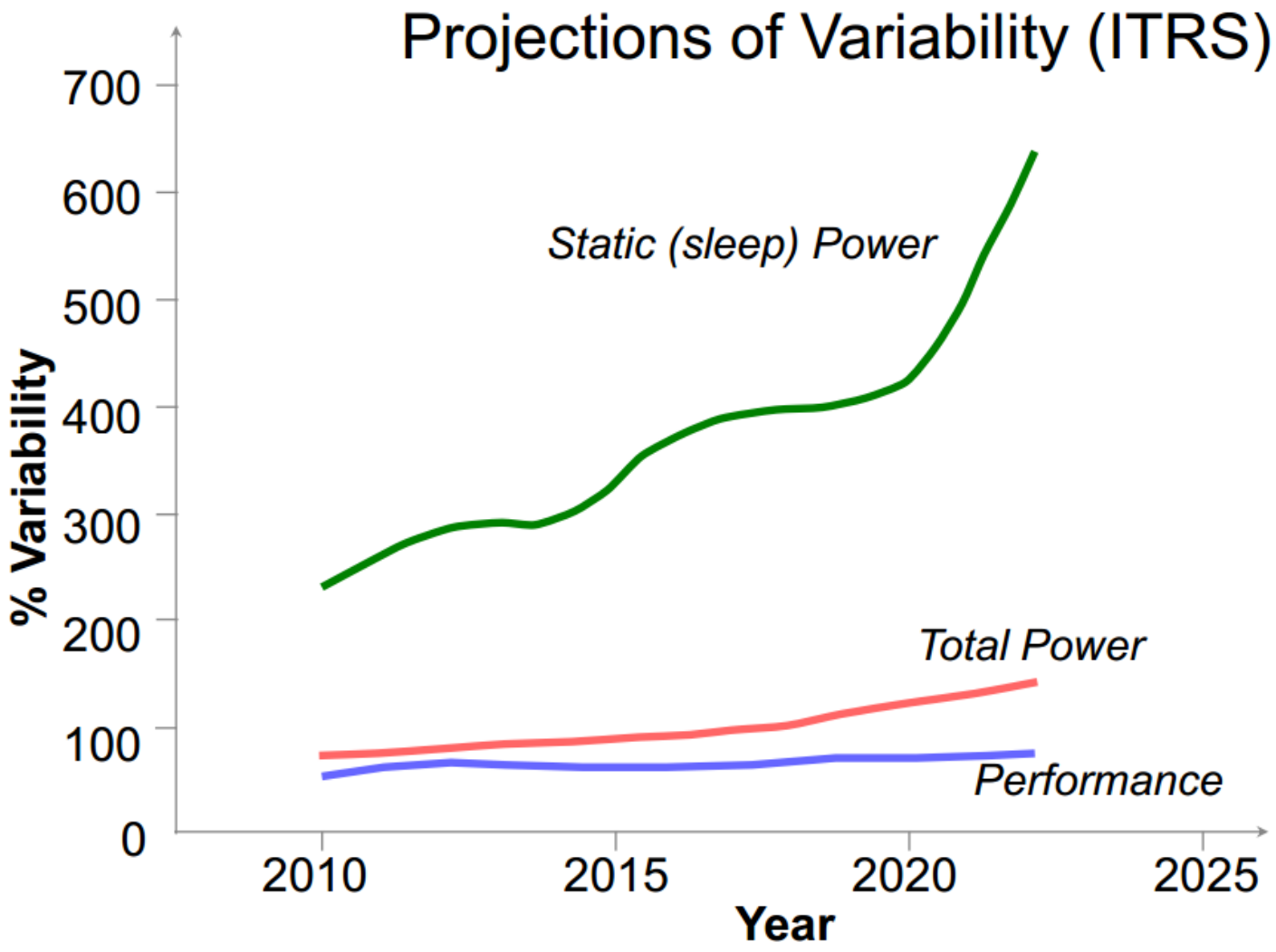
Variability Primer



Across wafer frequency variation

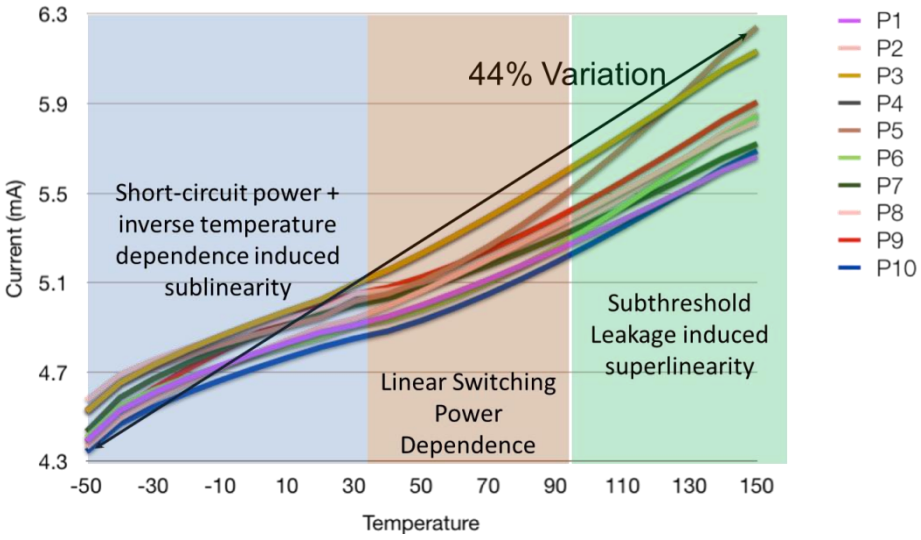
- Conservative guard bands
  - Consistent performance
  - Hardware is under-utilized
- Variability Mitigation
  - Adaptive Body Biasing
  - Error Correction
  - Aggressive binning

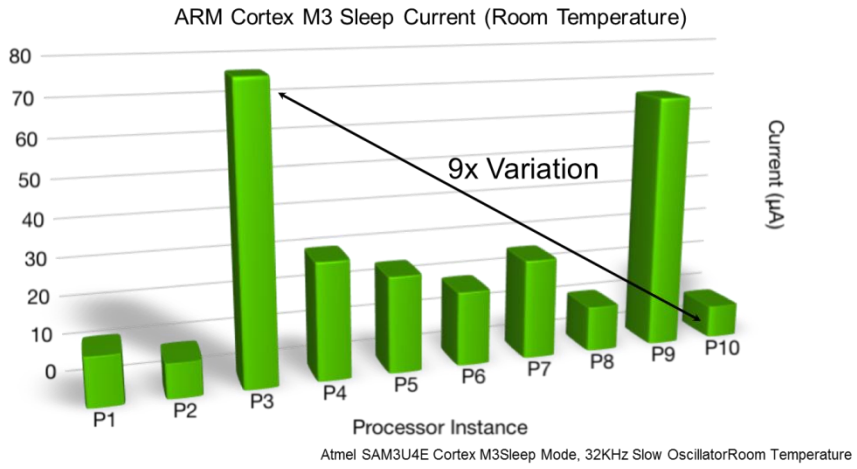
Variability Expected to Increase

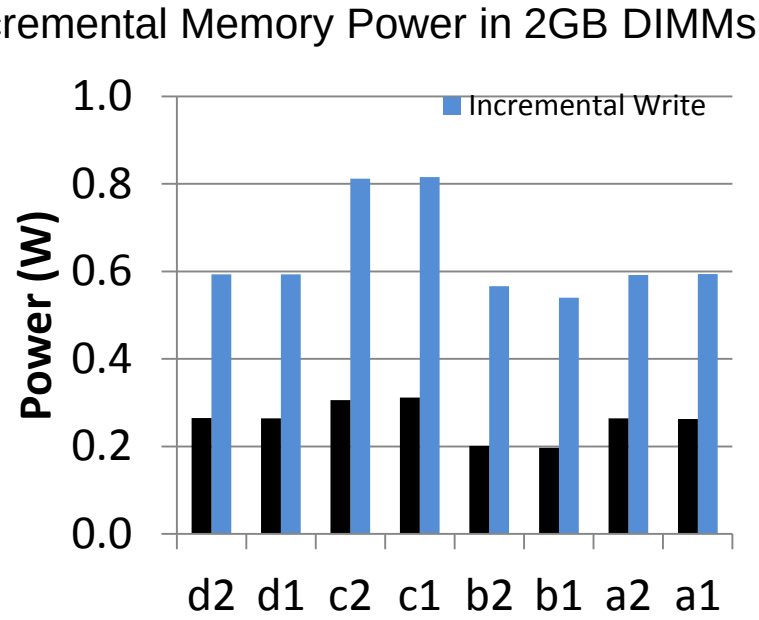


Ref: A Case for Opportunistic Embedded Sensing In Presence of Hardware Power Variability - L. Wanner, C. Apte, R. Balani, P Gupta, and M Srivastava

Measured Variability







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1: A Case for Opportunistic Embedded Sensing In Presence of Hardware Power Variability - L Wanner, C Apte, R Balani, P Gupta, and M Srivastava

2. ViPZonE: OS-Level Memory Variability-Driven Physical Address Zoning for Energy Savings – M Gottscho, L Bathen, A Nicolau, P Gupta, N Dutt

Why Processor Level Characterization?

- Motivation
  - Variability in real world applications
  - Impact of variability mitigation techniques
  - Effectiveness of binning strategy
- Challenges
  - Complex architecture
  - Power saving strategies like C-States
  - DVFS strategies like Turbo Boost
- No public data available to study system-level variation

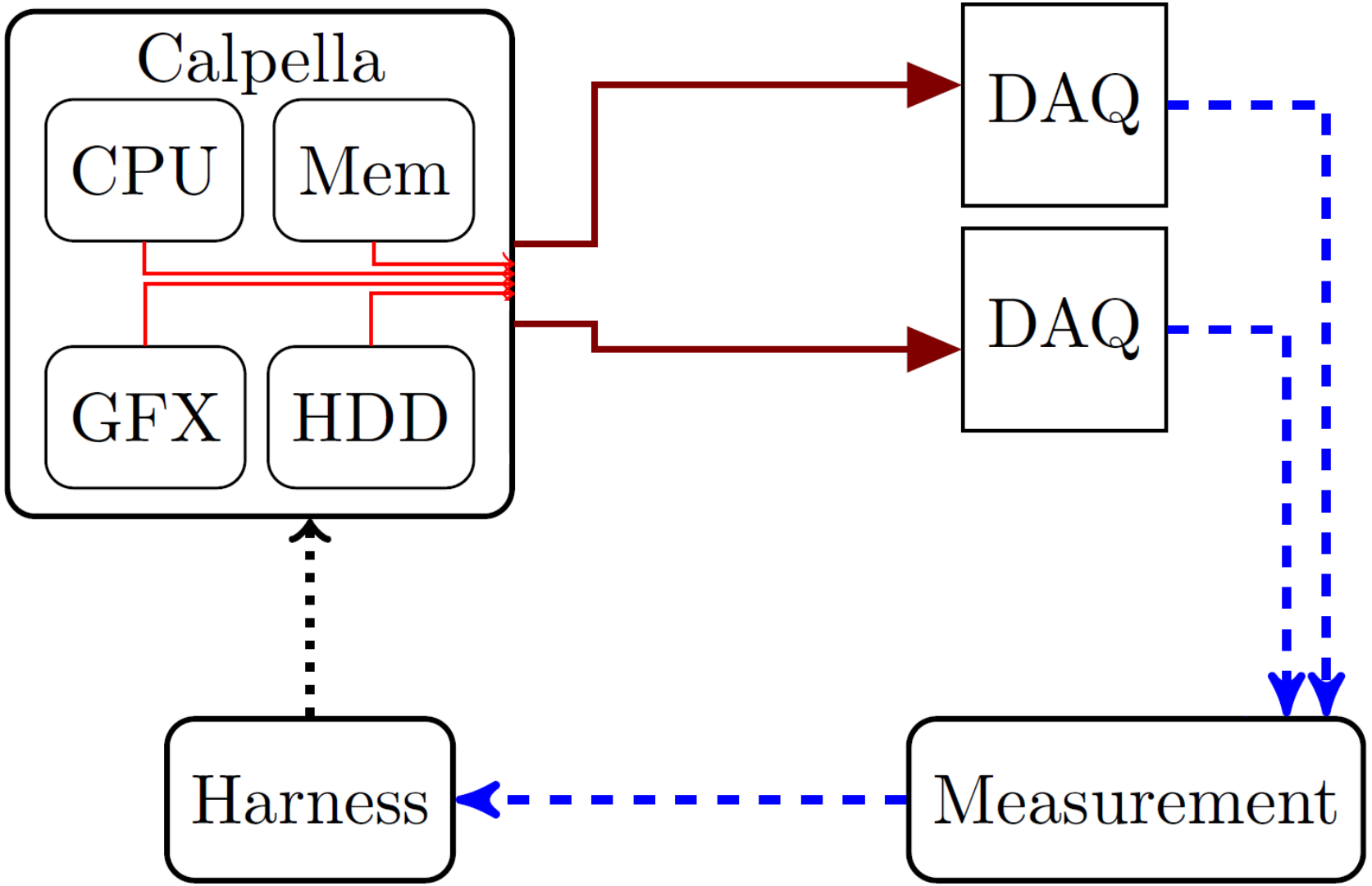
Outline

- Motivation
- Measurement Setup
- Results
- Implications & Future Work

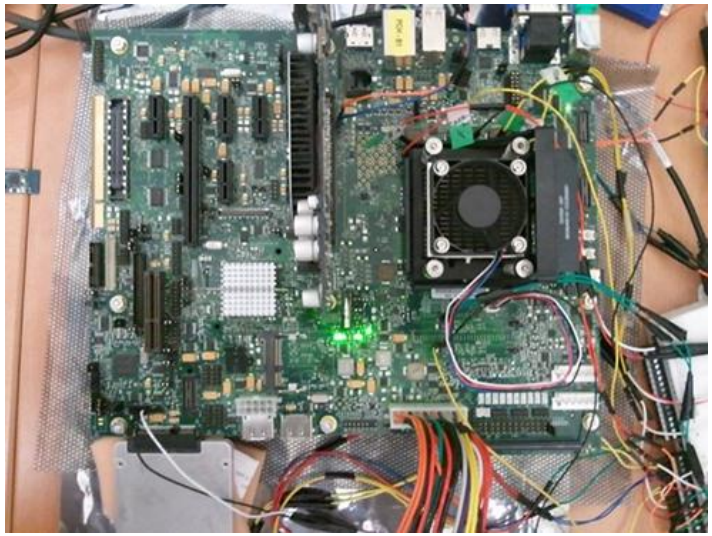
Mobile Processor Characterization

- 6 x Core i5-540M processors
  - Nehalem class, Dual Core
  - 32nm processor
  - 35W thermal design power
  - Frequency: 1.20 GHz - 2.53 GHz
  - Turbo Boost 1.0 (3.06GHz)
  - C-States (sleep states) support up to C6
  - Hyper-Threading

Measurement Setup



Measurement Setup



- Calpella: only CPU core
- Linux kernel
- NI DAQ: 16 bit, 1ms
- BIOS options:
  - Turbo Boost, Hyper-Threading, C-States
- Test Harness
  - Frequency control: userspace cpu governors
  - Core affinity: Linux cpuset

Measurement Challenges

- Several factors can affect measurements:
  - Operating Systems, Thermal, Transient, ..
- To eliminate these causes:
  - Transients: Multiple iterations of each benchmark
  - OS effects: System Reboot for every set of runs
  - Thermal: Processors swapped in and out of socket
- All variations shown as standard deviation
- Verify results across identical platforms

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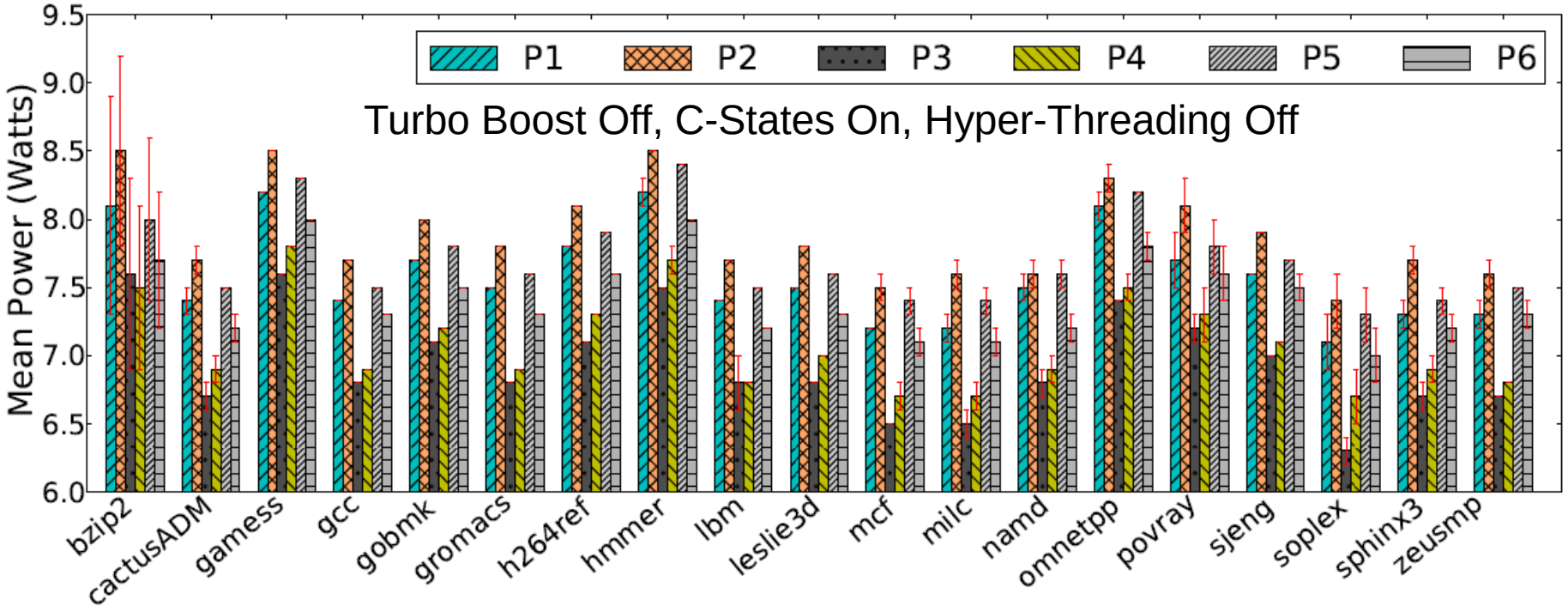
Results Outline

- Power Variation:

$$\frac{\text{Max } P_{avg} - \text{Min } P_{avg}}{\text{Min } P_{avg}}$$

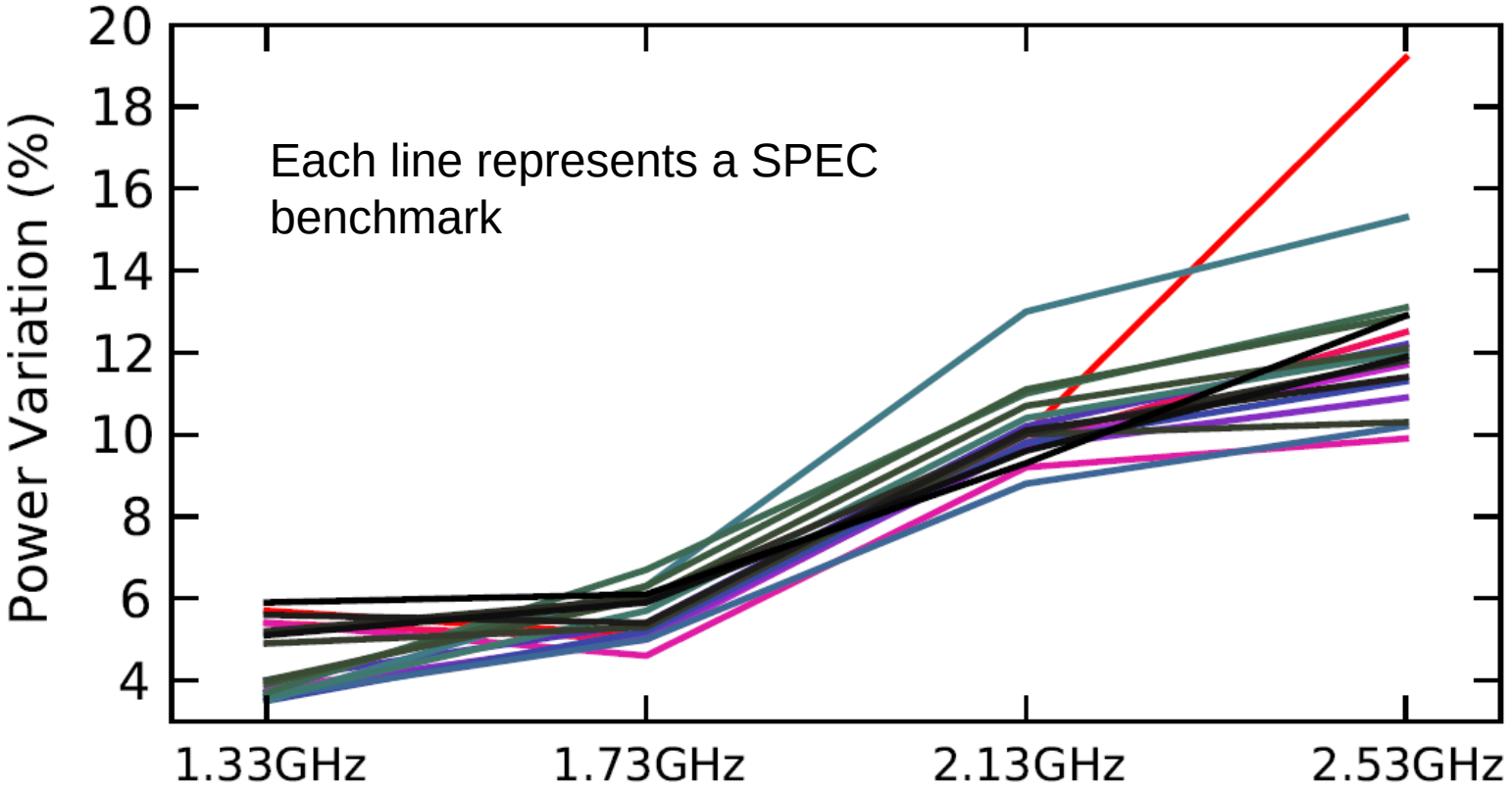
- SPEC:
  - Representative 19 out of 36 benchmarks
  - Config: P-States, Turbo Boost, C-States
- PARSEC:
  - 12 out of 13 benchmarks
  - Config: Hyper-Threading, Turbo Boost

Power Measurements



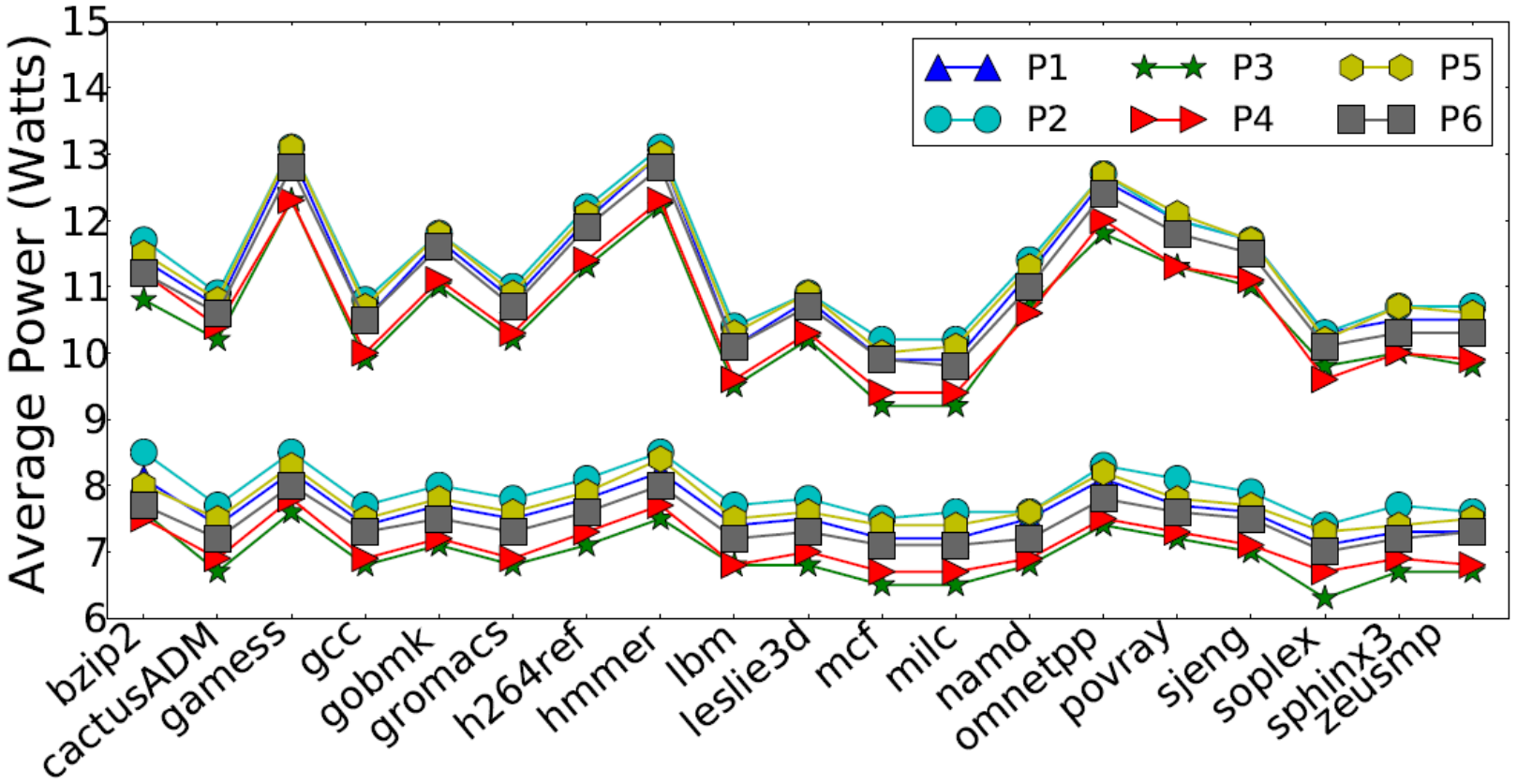
- Ordering of processors same for all benchmarks
- Power Variation of 12% - 17% across benchmarks

Variation with P-States



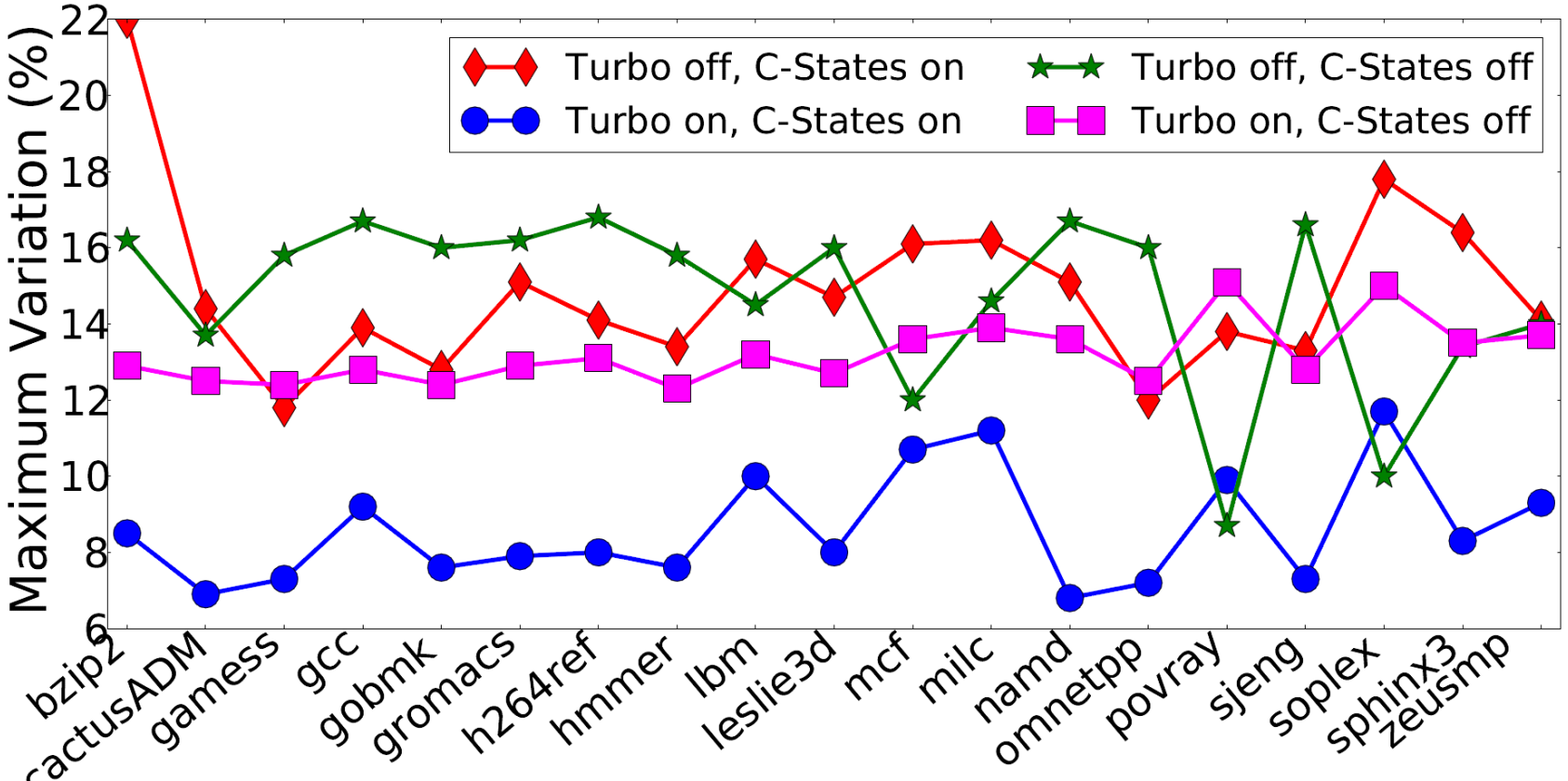
- Variation increases with frequency
- E.g. sphinx3: 1.33GHz 5.9%, 2.53 GHz 16.4%
- Cause: Leakage power increases with P-State

Effect of Turbo Boost: On and Off



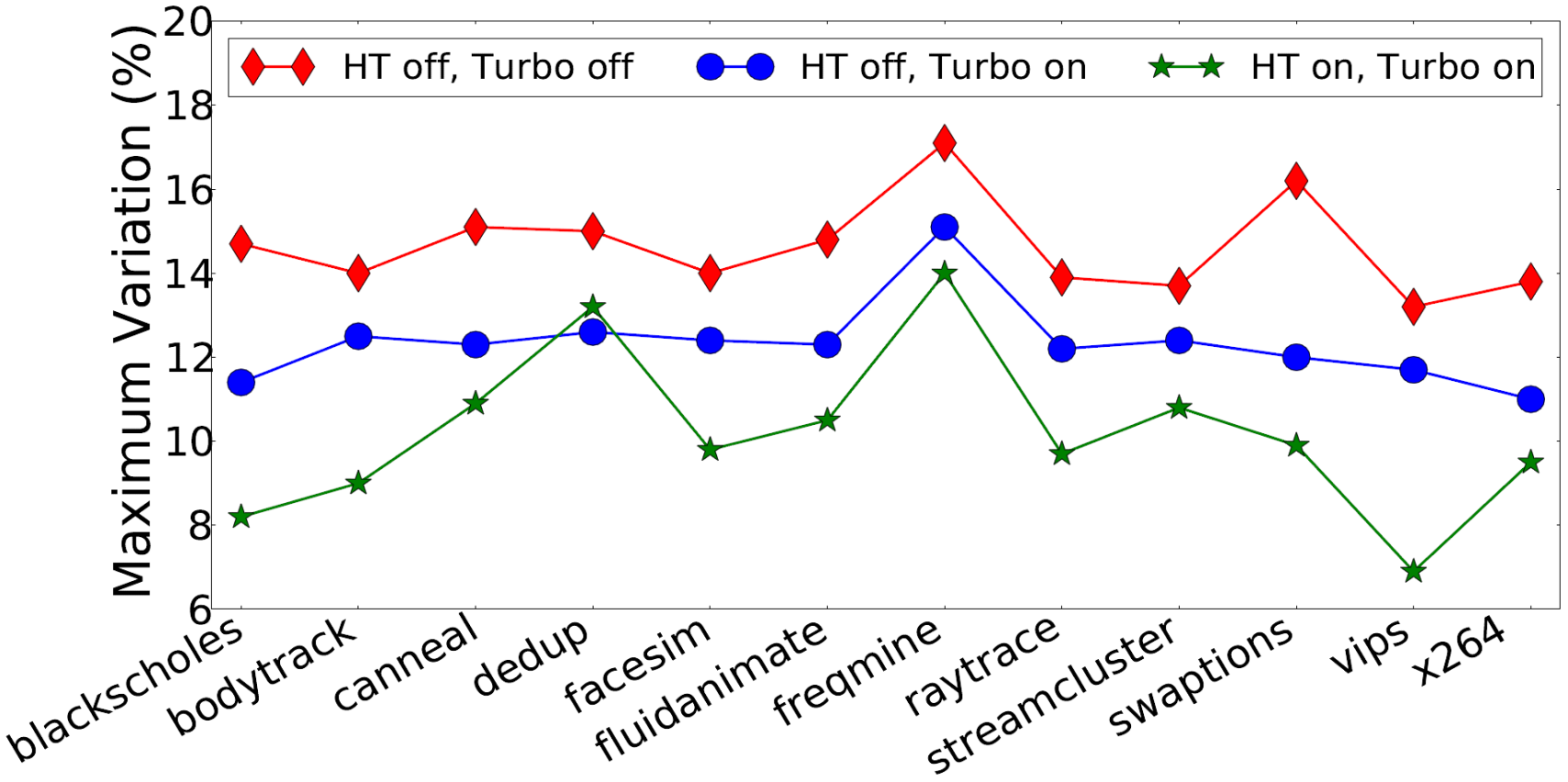
- Power and performance increase
- Turbo Boost On, C-State On: 7-12% variation
- Cause: Shut down of unused cores

Variation: Turbo Boost & C-States



- Variation increases with Turbo Boost disabled
- Variation increases with C-states disabled
- Cause: Leakage current increase with C-state Off

Mutli-threaded Benchmarks (Parsec)



- Variation decreases with Turbo Boost and HT
- Cause: Disabled HT circuits and drop in frequency

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Implications

- Leakage power is the dominant cause of variation
- Variability in processor, memory and SSD
  - Battery lifetime will vary between instances
  - Modeling of power is harder with variation*
- We observe low within-die variation

*Ref: Evaluating the Effectiveness of Model-Based Power Characterization. John C. McCullough, Yuvraj Agarwal, Jaideep Chandrashekar, Sathyanarayan Kuppuswamy, Alex C. Snoeren, and Rajesh K. Gupta

Future Work

- Investigate Causes
  - Model-specific registers (MSRs)
- Characterization of other class of processors
  - Architectures: Sandy Bridge, Ivy Bridge
  - Platforms: Servers, Cell Phones
- Models of system-level variability

Conclusion

- Power Variation: 7% to 17% (2.53Ghz)
- Variation increases with frequency
- Variation increases with Turbo Boost disabled
- Variation increases with C-States disabled
- Variation increases with HT disabled
- Leakage power causes variation

- Dataset released:
  http://mesl.ucsd.edu/site/pubs/HotPower12_dataset.tgz

Questions?

http://www.variability.org