PHMon: A Programmable Hardware Monitor and Its Security Use Cases

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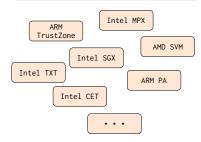


Motivation Overview

Motivation

Current Trend

• Growing demand to enforce security policies in hardware



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Current Trend • Growing demand to enforce security policies in hardware MPX SafeC Softbound Available Intel MPX 2008 2013 2018-2019 ARM TrustZone G G G 6 ٢h AMD SVM 1994 2009 2015 Intel SGX Hardbound MPX MPX Intel TXT Disabled Announced ARM PA Intel CET . . .

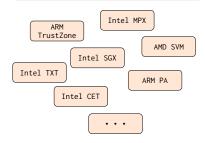
[AUSTIN, PLDI'94] [DEVIETTI, ASPLOS'08] [NAGARAKATTE, PLDI'09]

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Current Trend

• Growing demand to enforce security policies in hardware



What if

we could have a flexible hardware implementation that could enhance and enforce a variety of security policies as security threats evolve?!

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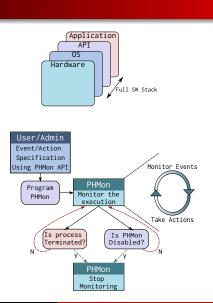
Our Proposal - PHMon

PHMon

- A hardware monitor and the full software stack around it
 - A programmable hardware monitor interfaced with a RISC-V Rocket processor on an FPGA
 - OS support
 - Software API
 - Security use cases

How Does It Work?

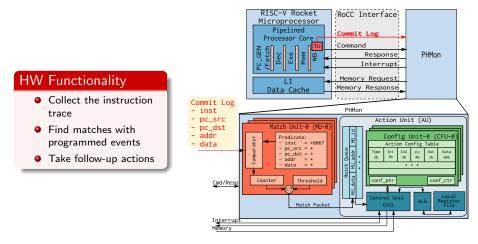
- A user/admin configures the hardware monitor
- The hardware monitor collects the
 - runtime execution information
 - Checks for the specified events, e.g., detects branch instructions
 - Performs follow-up actions, e.g., an ALU operation



Hardware

Software Implementation Use Cases

Hardware Overview



Hardware Software Implementation Use Cases

Software Overview

Software Interface

- A list of functions that use RISC-V's standard ISA extension
 - Configure PHMon
 - Communicate with PHMon

Reset MU-0 and configure the match pattern

phmon_reset_val(0);
phmon_pattern(0, &mask_inst0)

Compare pc_dst and pc_src, and trigger an interrupt

action_mu0.op_type = e_OP_ALU; //ALU operation action_mu0.in1 = e_IN_DATA_RESP; //MU_resp action_mu0.in2 = e_IN_LOC3; //Local3 action_mu0.fn = e_ALU_SEQ; //Set Equal action_mu0.out = e_OUT_INTR; //Interrupt reg phmon_action_config(0, &action_mu0);

OS Support

- Per process OS support
 - Maintain PHMon information during context switches
- Interrupt handling OS support
 - Delegate interrupt to OS
 - Terminate the violating process

Hardware Software Implementation Use Cases

Implementation and Evaluation Framework

Implementation

- PHMon as a RoCC, written in Chisel HDL
 - Interfaced with the in-order RISC-V Rocket core
- Linux kernel v4.15
- RISC-V gnu toolchain for cross-compilation

Evaluation

- Prototyped on Xilinx Zynq Zedboard
 - Rocket core + PHMon
- Open-sourced at https://github.com/bu-icsg/PHMon

Hardware Software Implementation **Use Cases**

Use Cases

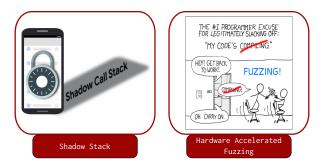


https://security.goglebiog.com/2015/14/protecting-againt-code-reuse-in-linu38.html, https://ww.dsreading.com/attack-breaches/heartbled-attack-targetd-enterprise-upn-/d/d-id/1204592, https://wedium.com/ddiseasytoofast/fuzing-and-deeplearning-5aae84c20303, https://hackernon.com/professional-debuging-in-rails-lyzbar

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Hardware Software Implementation **Use Cases**

Use Cases



https://security.googleblog.com/2019/10/protecting-against-code-reuse-in-linux30.html, https://medium.com/@dieswaytoofast/fuzzing-and-deep-learning-5aae84c20303,

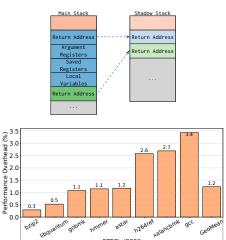
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Hardware Software Implementation **Use Cases**

Use Cases: Shadow Stack

PHMon-based Shadow Stack

- Simple and flexible
 - Two MUs
 - Shared memory space
 - Allocated by OS as a user-space memory
- Secure
- Efficient
 - For SPECint2000, SPECint2006, and MiBench benchmarks, on average, 0.9% performance overhead



SPECint2006

Hardware Software Implementation **Use Cases**

Use Cases: Hardware Accelerated Fuzzing

American Fuzzy Lop (AFL) [Zalewski, 2013]

- A state-of-the-art fuzzer
- Two main units
 - The fuzzing logic
 - The instrumentation suite
 - Compiler-based
 - QEMU-based



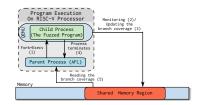
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Hardware Software Implementation Use Cases

Use Cases: Hardware Accelerated Fuzzing

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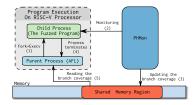
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QEMU-based AFL



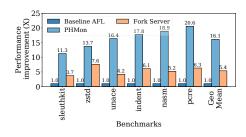
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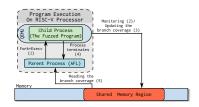


PHMon-based AFL

Hardware Software Implementation Use Cases

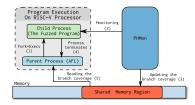
Use Cases: Hardware Accelerated Fuzzing





QEMU-based AFL

- PHMon improves AFL's performance by 16× over the baseline
- Power overhead: 5%
- Area overhead: 13.5%



PHMon-based AFL

Conclusion



A hardware monitor with full software stack





FPGA prototype



https://www.usenix.org/system/files/ sec20spring_delshadtehrani_prepub.pdf



https://github.com/bu-icsg/PHMon



Thanks! You can reach me at delshad@bu.edu for follow-up questions.

More information

Boston University