Coco: Co-Design and Co-Verification of Masked Software Implementations on CPUs

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2021-05-20

USENIX Security '21

IAIK – Graz University of Technology

Physical Side-Channel Attacks

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  - Microprocessors

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- Attacker:
  - Has physical access to device
  - Can observe or manipulate its physical properties, e.g. power consumption

Masking

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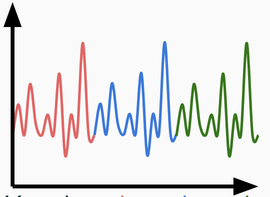

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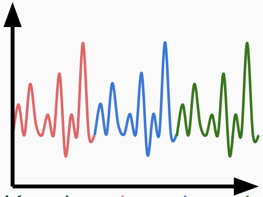
- Verification: Check separation of shares
  1. Algorithmically
  2. In a hardware circuit



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The HW/SW Gap

- So far, formal proofs for masked cryptography exist either:
  - For masked HW circuits (REBECCA[Bloem, 2018])
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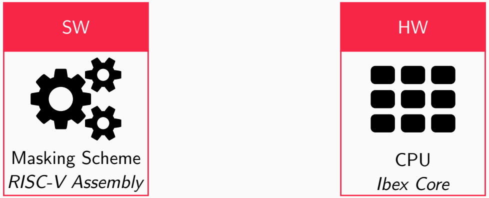

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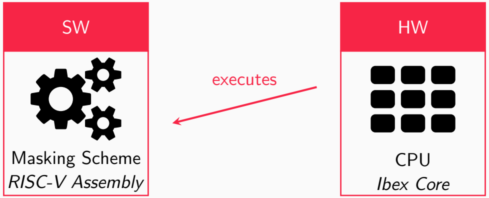

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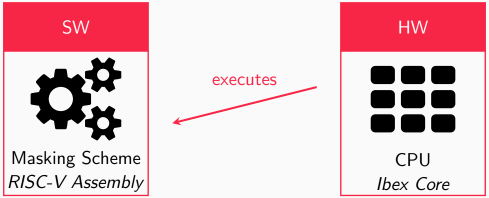

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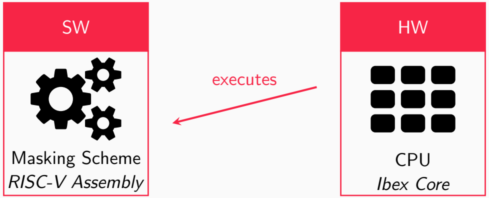

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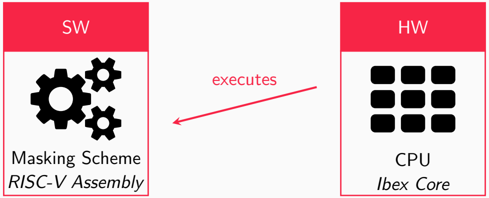

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  1. Detect leakage of a given masked SW implementation when executed on a given CPU netlist
  2. Construct SCA-hardened CPU components

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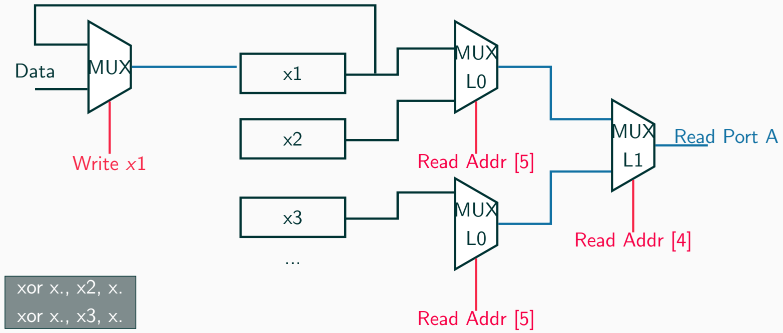

xor x., x2, x.
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Co-Verification Flow of Coco

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RISC-V Assembly

HW

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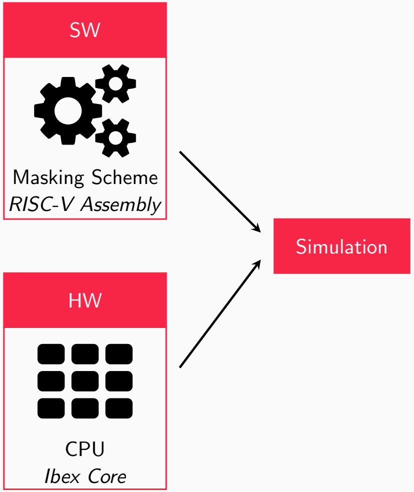

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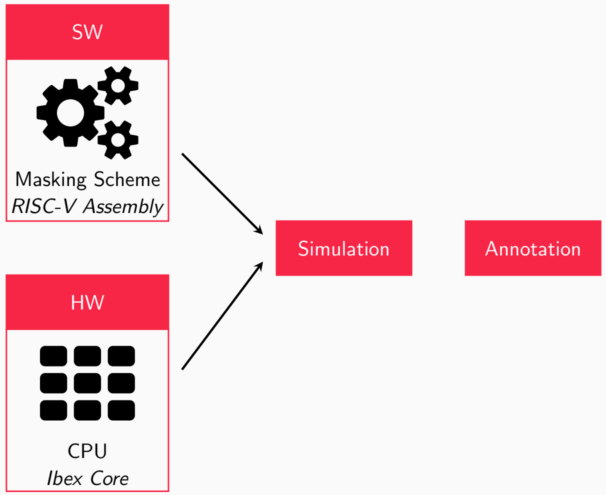

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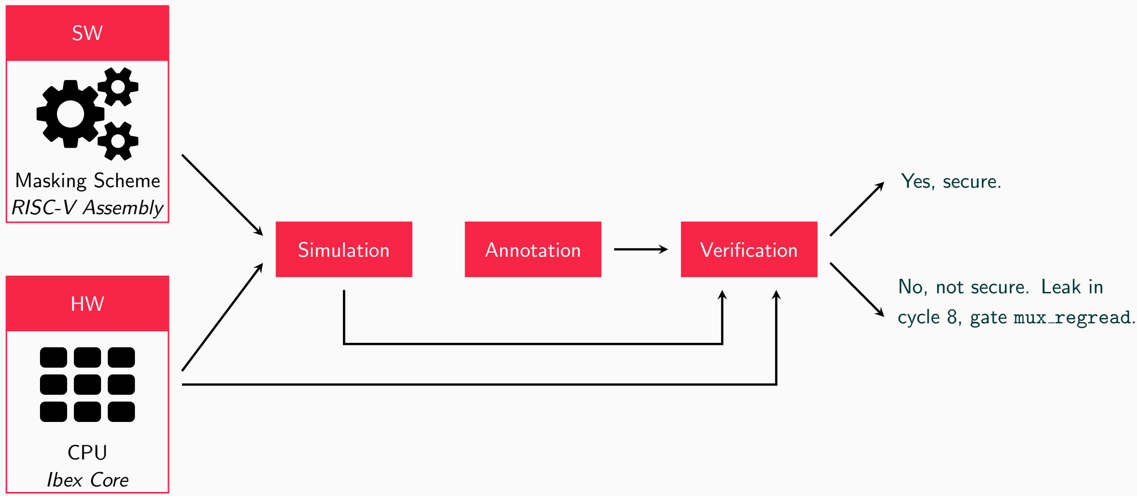

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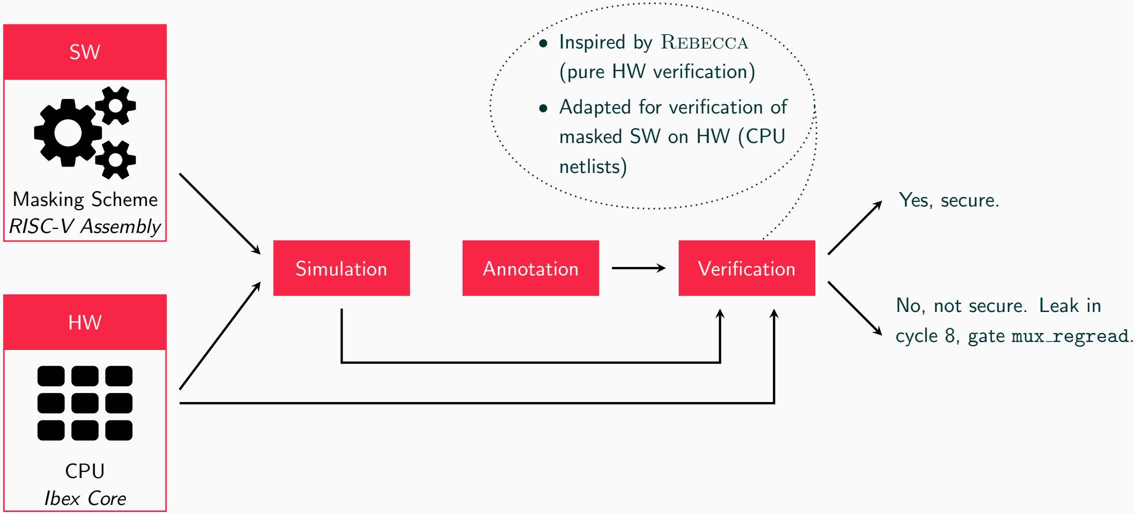
SW
Masking Scheme
RISC-V Assembly
HW
CPU
Ibex Core
Simulation
Annotation
Verification
Inspired by REBECCA (pure HW verification)
Adapted for verification of masked SW on HW (CPU netlists)
Yes, secure.
No, not secure. Leak in cycle 8, gate `mux_regread`.

Co-Design with Coco

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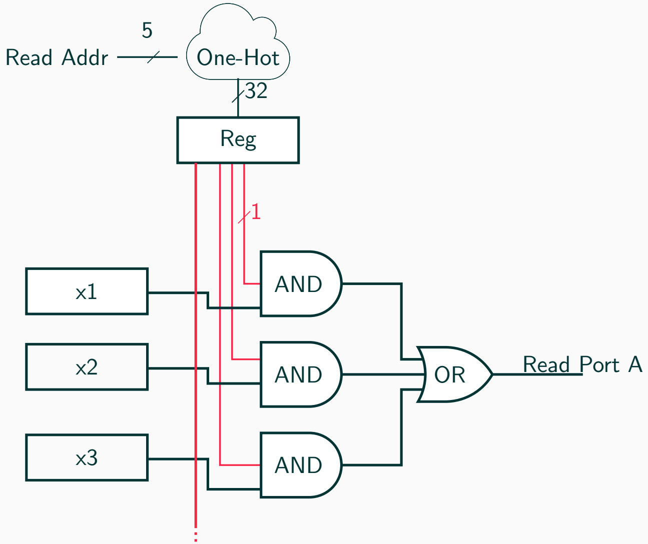
- Case-study: RISC-V Ibex core
  - 32-bit, 2-stage pipeline, in-order, single-issue
- Hardening Ibex with Coco
  - Reported leaks in register file, computation units (ALU, Multiplier, CSR Unit), Load-Store Unit, data memory
  - Solution: (1) Hardware fixes and (2) Software Constraints

Example: Hardened Ibex Register File

- Original register file had several problems:
  - Switching wires in multiplexer tree
  - Glitchy address signals
  - Unintended reads



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