33RD USENIX
SECURITY SYMPOSIUM

SpecLFB: Eliminating Cache Side Channels in Speculative Executions

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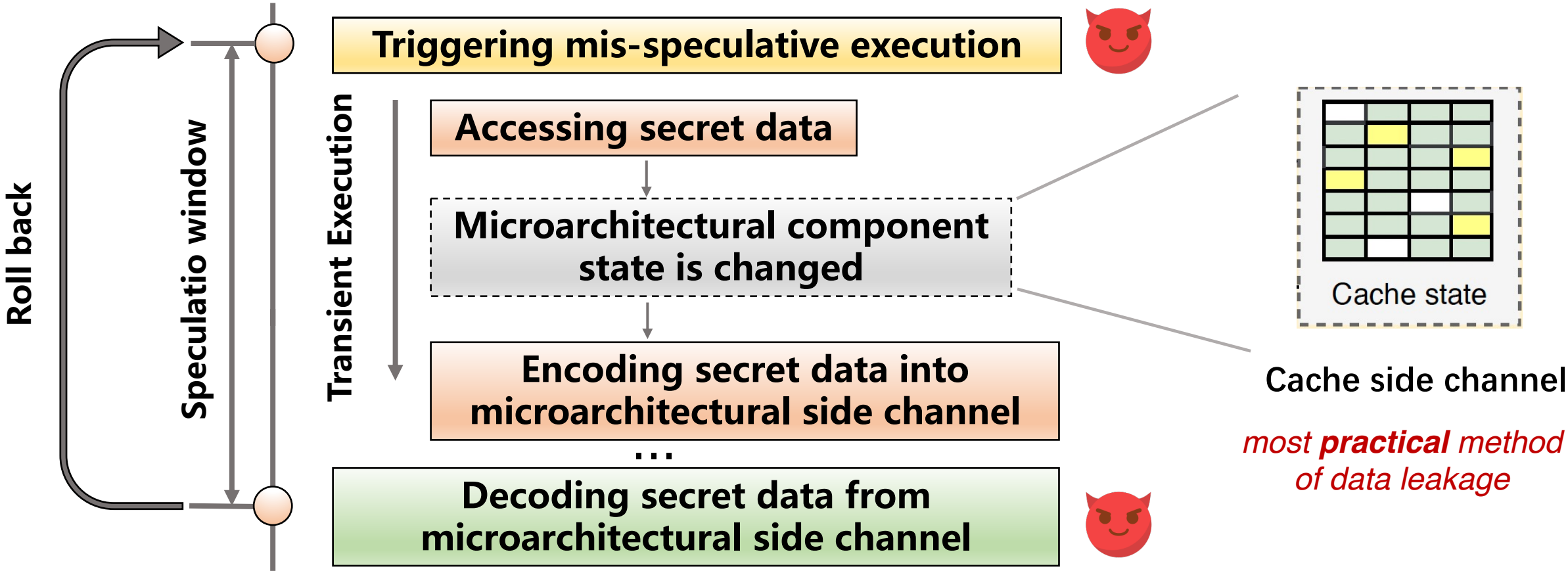
Presented at USENIX Security 2024

Contents

Spectre Attack

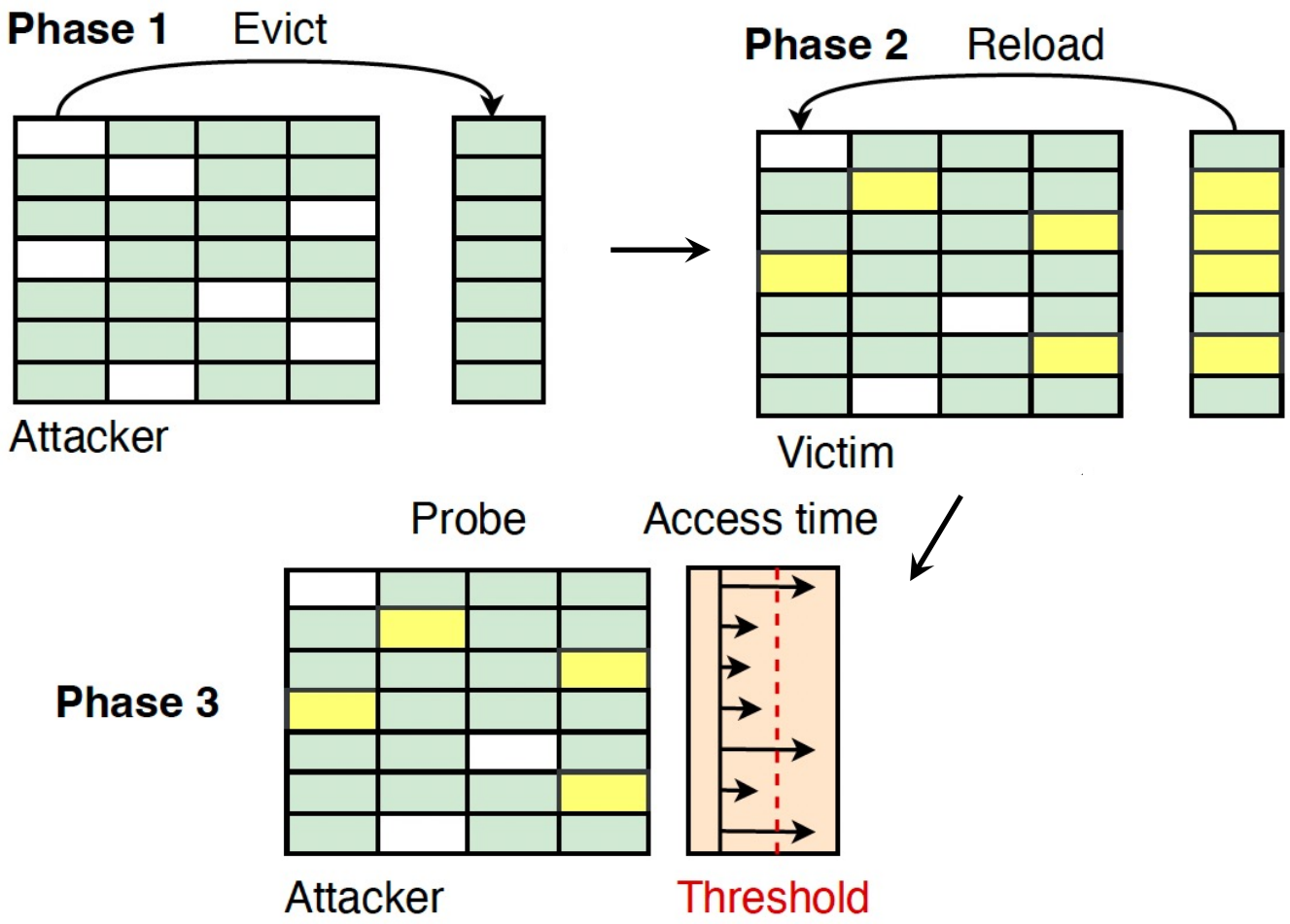


Spectre v1 [S&P' 19]

```
if (x < array1_size)
    y = array2[array1[x] * 4096];
```

Secret byte

Cache Side-channel Attack



Flush-Based Attack:

An attacker uses specialized machine instructions, such as the x86 CLFLUSH instruction used in Flush+Reload [USENIX Security'14], to flush the target cache line.

Flush+Flush [DIMVA' 16]

Flush+Coherence [HPCA'18]

Reload+Refresh [USENIX Security'20]

Conflict-Based Attack:

An attacker constructs a conflict set to evict the target cache line.

Evict+Reload [USENIX Security'16]

Prime+Probe [S&P'19]

Prime+Abort [USENIX Security'19]

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Existing defense solutions

- Using serialization instructions within branches.
  - *Equivalent to completely disabling branch prediction*
- Invisible speculation

  InvisiSpec [MICRO'18] *SafeSpec* [DAC'19] *MuonTrap* [ISCA'20]
  - *Additional data structures to hide the cache lines accessed by the speculative loads*
  - *The data movement caused by the re-installing operations*
- Selective speculation

  STT [MICRO'19] *NDA* [ISCA'20] *SDO* [ISM'19] *SSE-RV* [CARRV'21]
  - *Complex tracking analysis logic*
  - *Untained technique cannot deprotect in time*
  - *A large taint file as a shadow structure for the PRF*

Problems

The combination of cache side-channel and speculative execution allows attackers to leak arbitrary data from the victim’s memory space

↓

Solutions

Sometimes block instructions without security threats

Require additional data structures and data movement operations, or complex logical implementation

→ **Significant overhead**

Most of the hardware defense solutions lack real hardware prototypes

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Threat Model

Focus on eliminating cache side channels in speculative execution established by **flush- and conflict-based cache side-channel** attacks, which **require pre-evicting the cache lines to be leaked.**

- Attackers are allowed to run arbitrary code before and during the victim's executions to affect the victim's speculation.
- Attackers are aware of the cache index method and re-placement strategy, enabling them to evict target cache lines from the cache.
- Attackers can locate gadgets within the victim's executable memory space.

Design concept

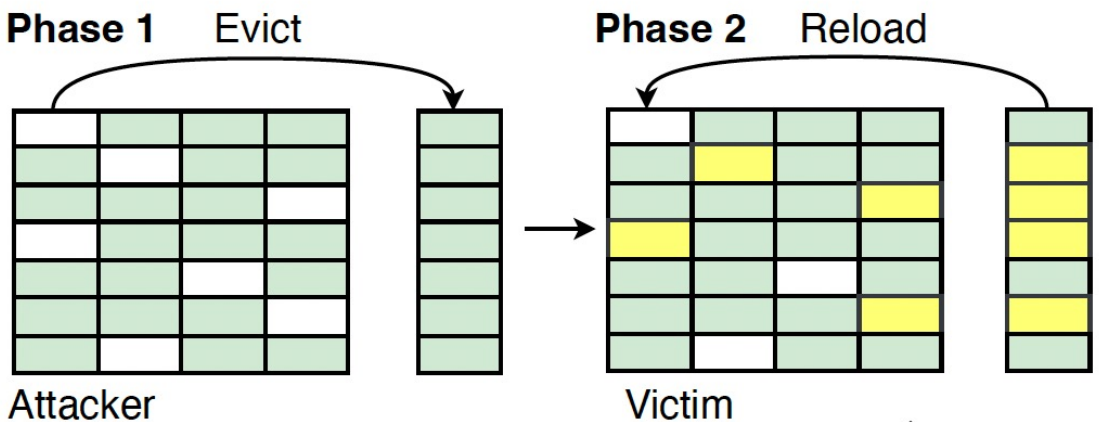
The larger the scope of protected instructions and the longer they are protected, the more dependent instructions will be blocked

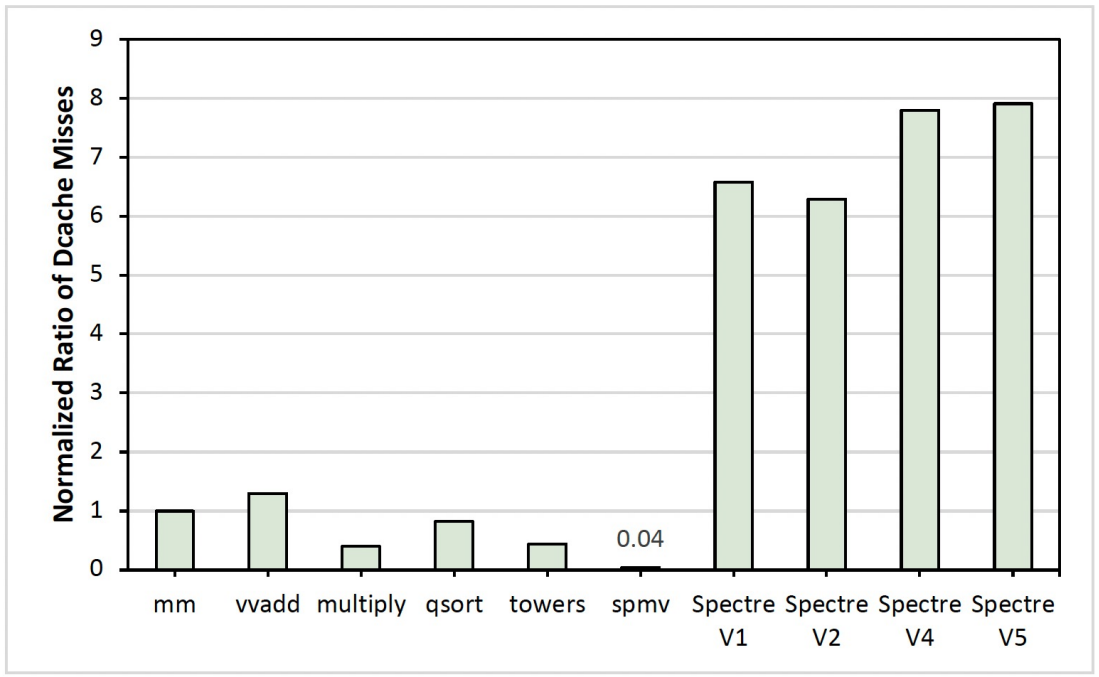
Protection scope **Which speculative loads should be protected?**

↓

All speculative loads could be exploited by attacker ?

Attack Characteristic Analysis





- *The cache lines that are exploited to leak data by the attacker must be under cache misses states in Phase 1.*
- *The victim's speculative loads which reload these cache lines thereby change the cache's occupancy state in Phase 2.*

The speculative loads causing cache misses are considered unsafe and should be protected.

Unsafe **S**peculative **l**oads caused cache **m**isses —— **MUSL**

Design concept

The larger the scope of protected instructions and the longer they are protected, the more dependent instructions will be blocked

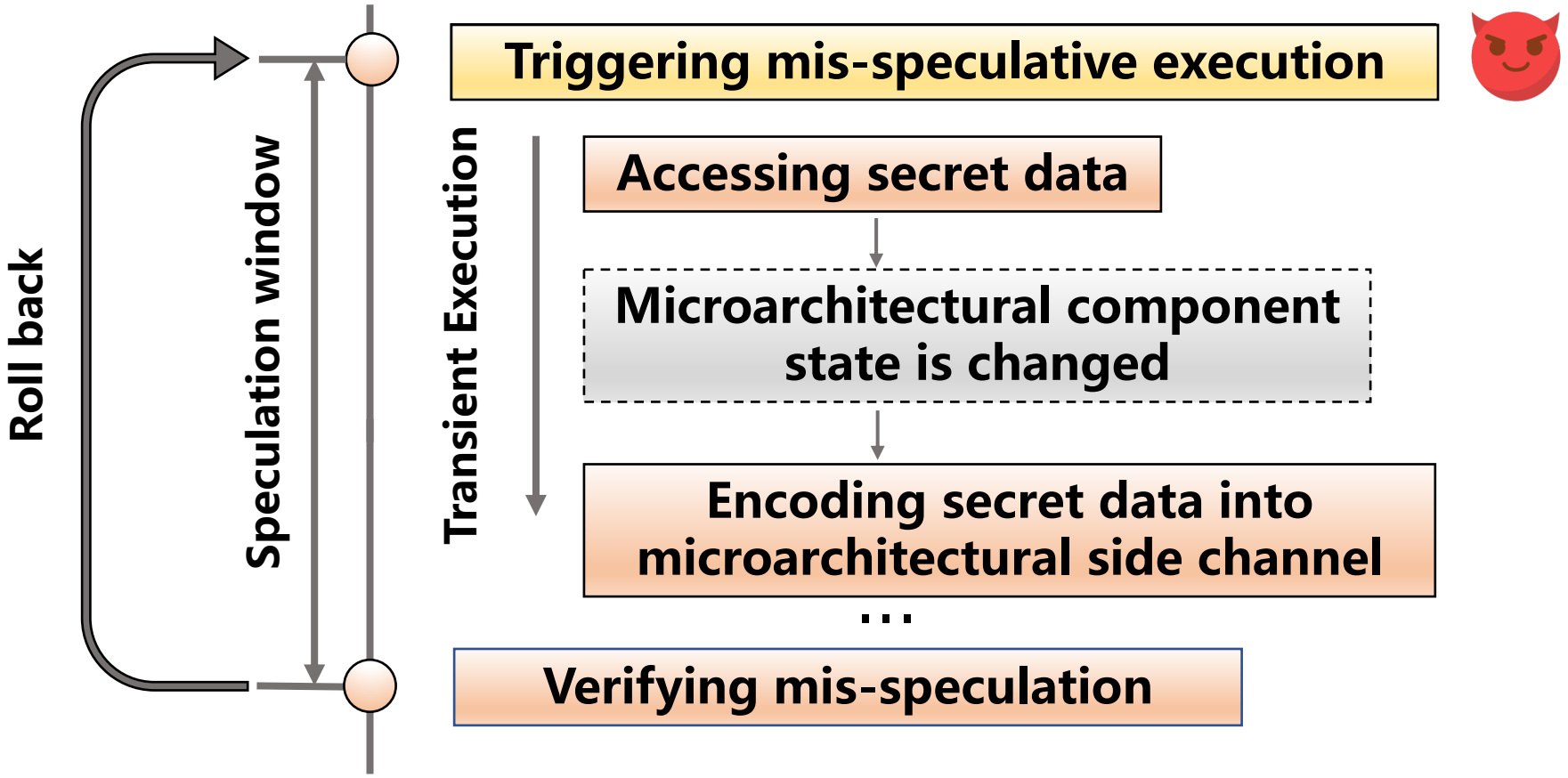
Protection scope — **Which speculative loads should be protected?**

↓

The speculative loads causing cache misses.

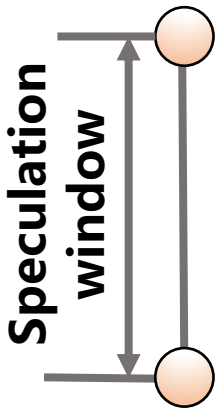
Protection duration — **When to protect and deprotect?**

Spectre Attack



Time to protect and deprotect

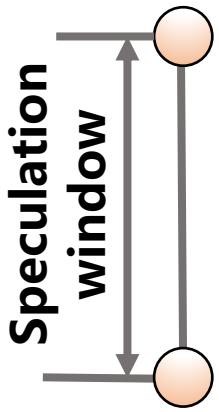
Unresolved Control Flow:



When control instructions (e.g. jumps, branches) enter the ROB

When the conditions and addresses can be verified by the processor

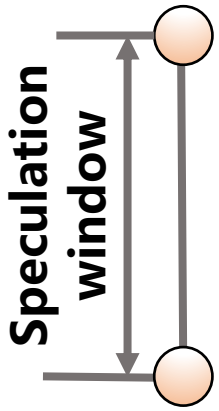
Unresolved Memory Access Order:



When stores with unresolved addresses enter the ROB

When the processor obtains the address of the store

Unresolved Value:



When the dependent instruction is executed using the predicted source operand value

When the predicted value can be verified by the processor

The loads within speculation window need to be protected

↓

The speculative loads under correct speculation need to be deprotected once the speculation window ends

Design concept

The larger the scope of protected instructions and the longer they are deprotected, the more dependent instructions will be blocked

Protection scope — **Which speculative loads should be protected?**

↓

The speculative loads causing cache misses.

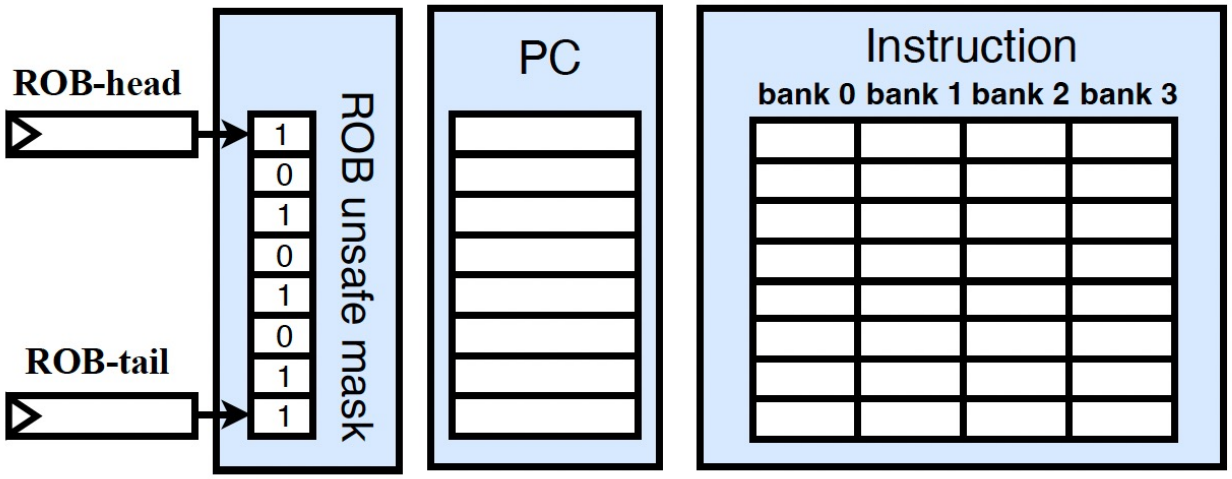
Protection duration — **When to protect and deprotect ?**

↓

Speculation windows caused by different speculation sources

Contents

ROB unsafe mask

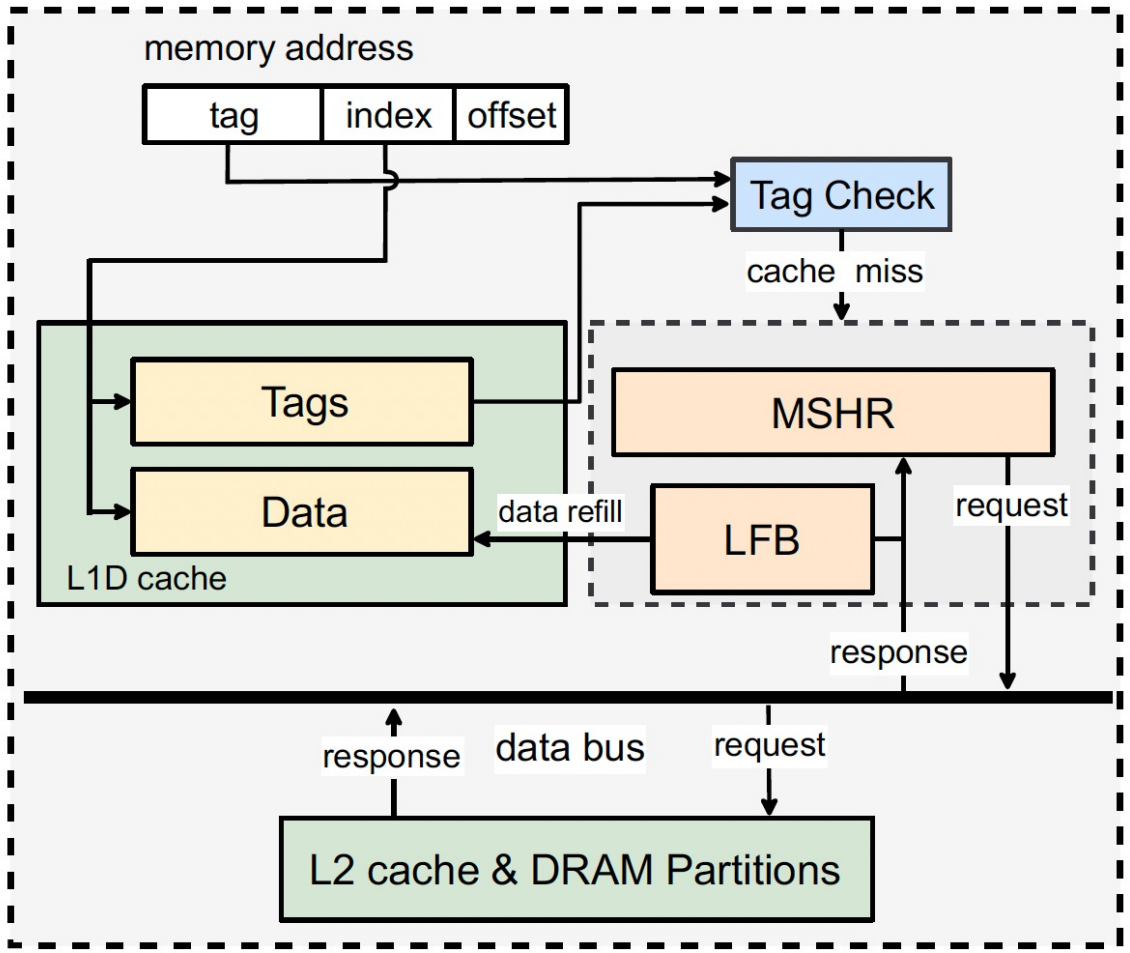


- *Each ROB rows are divided into multiple banks in multi-bank ROB architecture.*
- *Each entry of a bank stores the information of one µop.*
- *A one-to-one mapping exists between the ROB rows and the bits of ROB unsafe mask.*
- *The value of each bit in the ROB unsafe mask is jointly determined by the instructions in all banks of that ROB row.*

Number of ROB entries	M	
Number of banks	N	
ith bit of the ROB unsafe mask	r_i	$(i \in [0, M-1])$
jth bank of the ith entry of the ROB	b_{ij}	$(j \in [0, N-1])$

$$r_i = b_{i0} || b_{i1} || b_{i2} || \dots || b_{ij} || b_{i(N-1)}$$

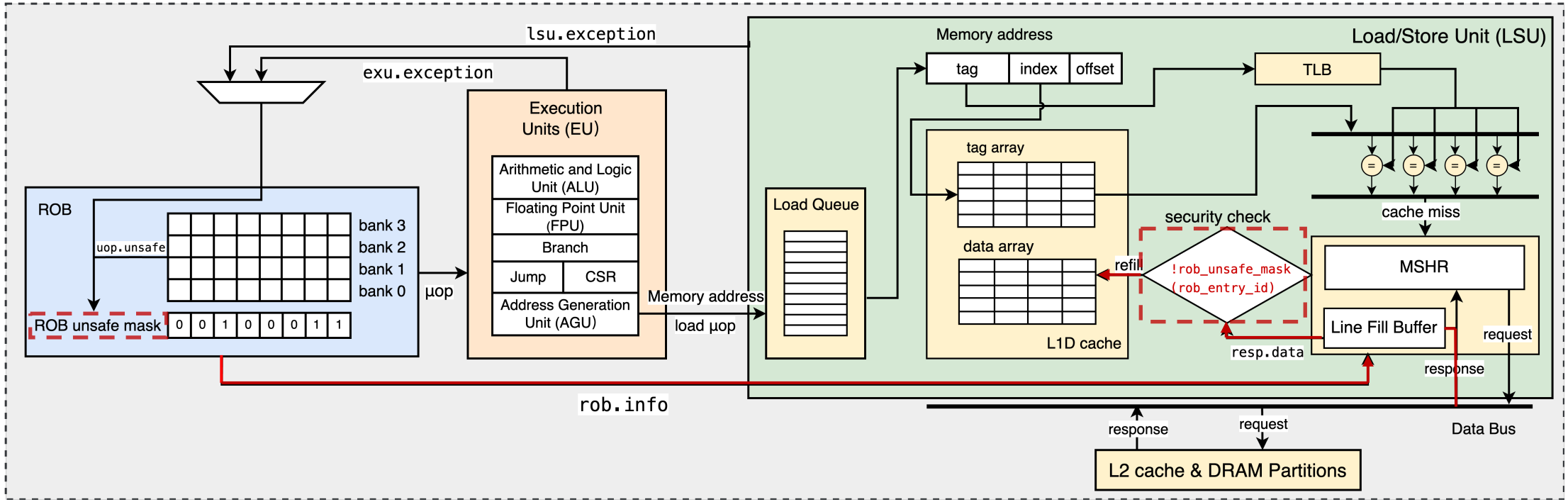
➢Line-fill-buffer (LFB)



Missing Status Holding Register (MSHR): Manages and sends data requests generated by cache misses to retrieve the missing cache line from lower-level caches or memory.

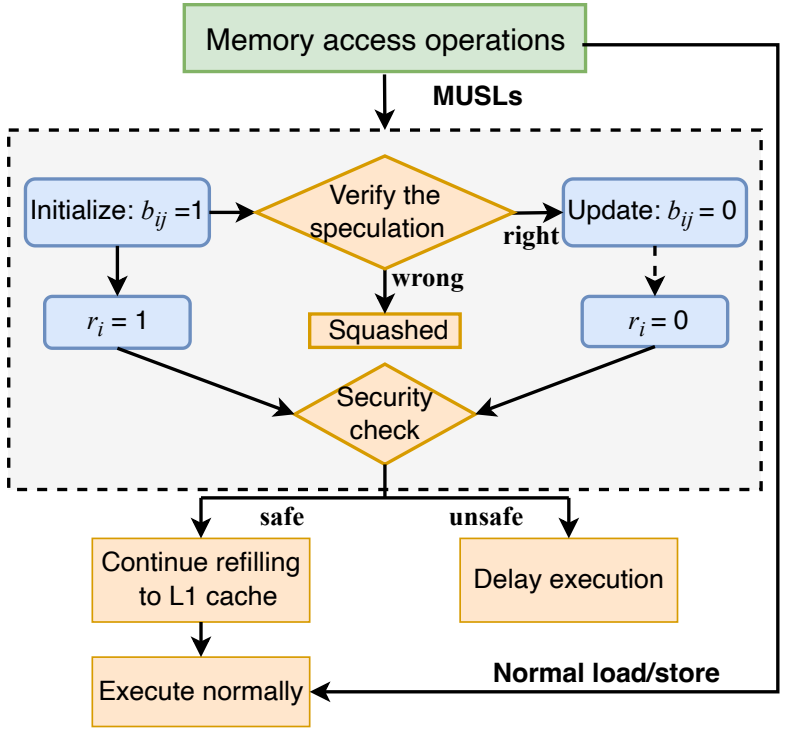
Line Fill Buffer (LFB): Temporarily stores retrieved cache lines by loads under cache misses, allowing cache eviction and refilling to occur in parallel, further reducing memory access latency caused by cache misses.

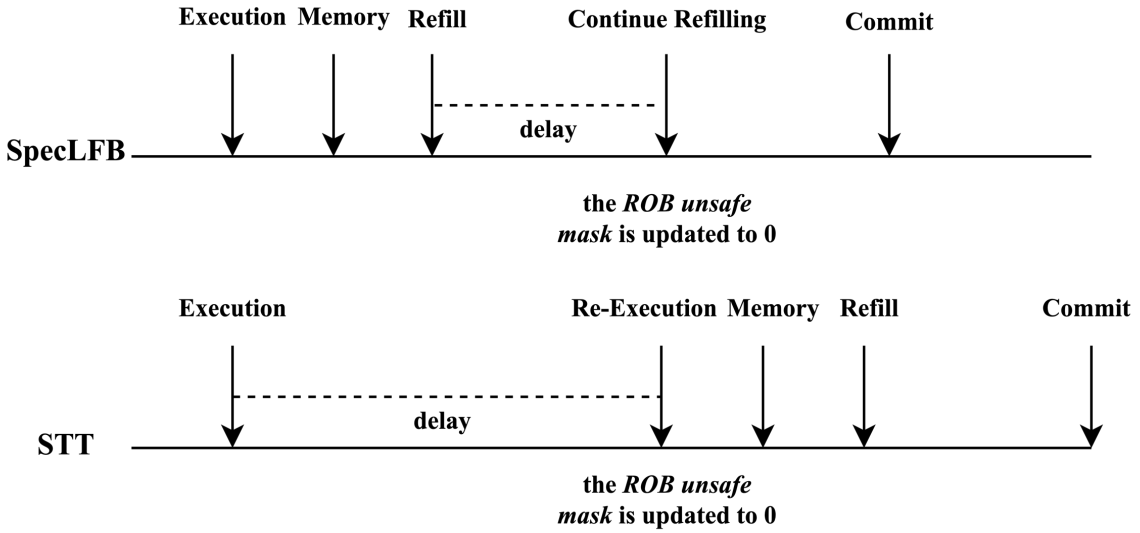
Security check mechanism



- The lower-level cache is requested by MSHRs to retrieve the missing data of loads under cache misses.
- The response data pass through the **security check mechanism** introduced to **LFB**.
- Only when the security check mechanism determines that the requested load is not a **MUSL**, can the data be **refilled into** the cache.

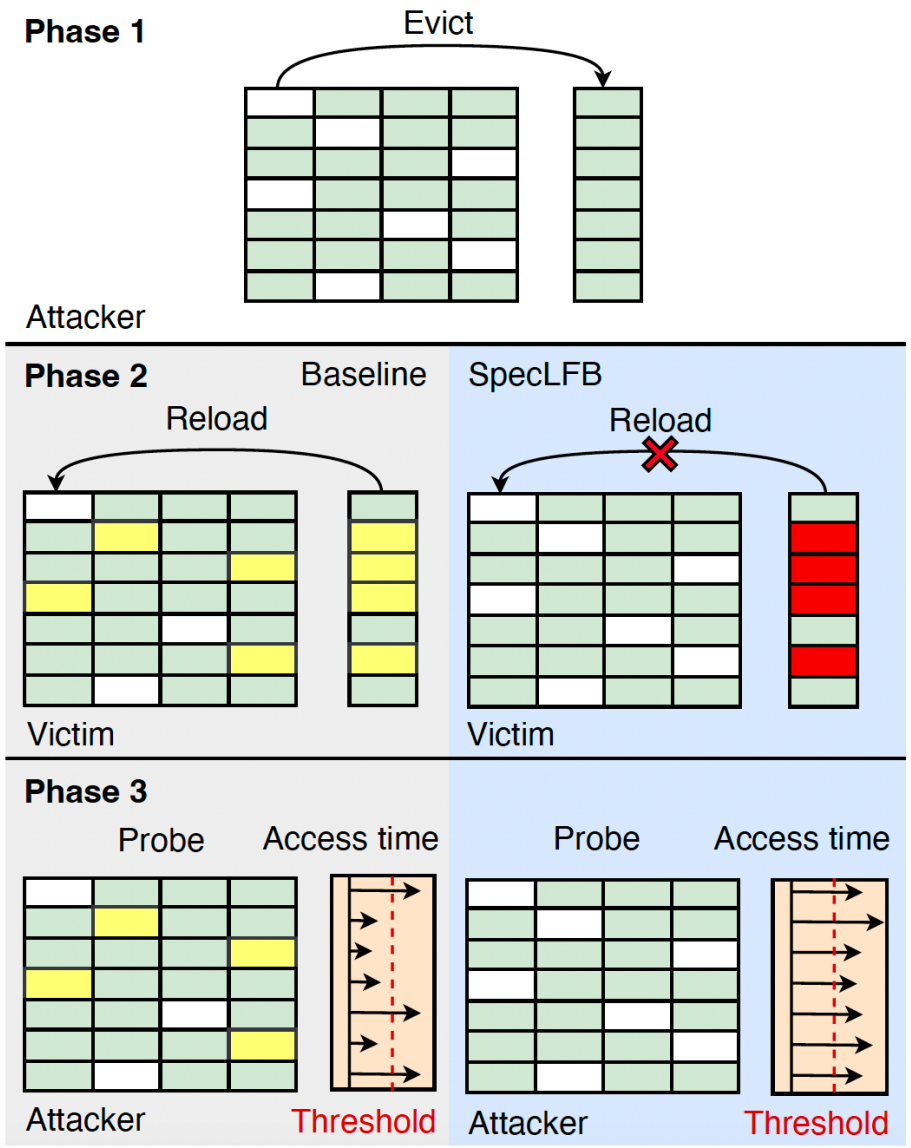
Security check mechanism





- During the waiting period for SpecLFB to update the ROB unsafe mask, the MSHR can simultaneously request data of MUSLs from the lower-level caches or memory
- As soon as the protection is disabled, the requested data can be refilled directly from the LFB into the cache instead of the lower-level caches or memory

SpecLFB Security Analysis



Phase 2:

Victim's load

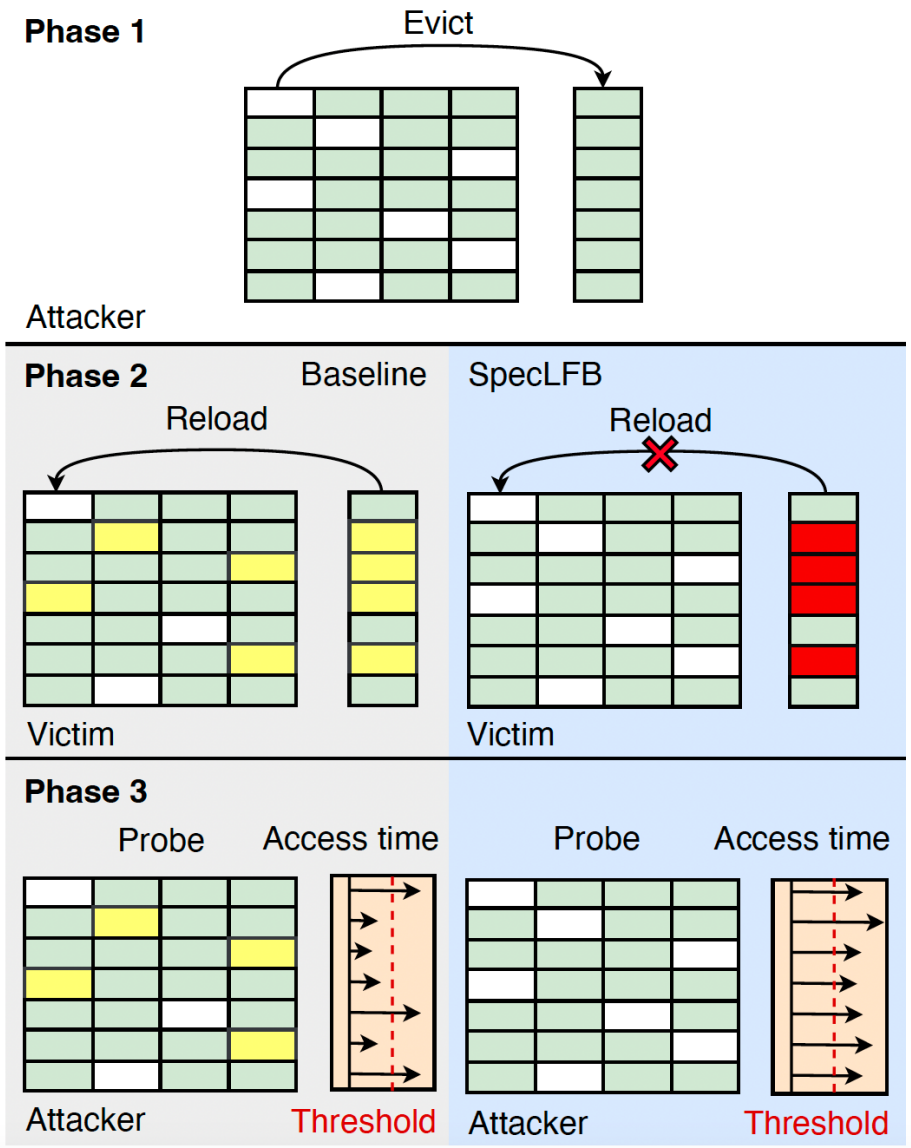
Is a cache miss generated? → **A cache refill occurs**

Is it within the speculation window? → **ROB unsafe mask bit is set to 1**

MUSL

*The cache lines requested by **MUSLs** cannot pass through the **security check in LFB** to be refilled into the cache*

SpecLFB Security Analysis



Phase 2:

Victim's load

Is a cache miss generated? → **A cache refill occurs**

Is it within the speculative window? → **ROB unsafe mask bit is set to 1**

MUSL

*The cache lines requested by **MUSLs** and cannot pass through the **security check in LFB** to be refilled into the cache*

Phase 3:

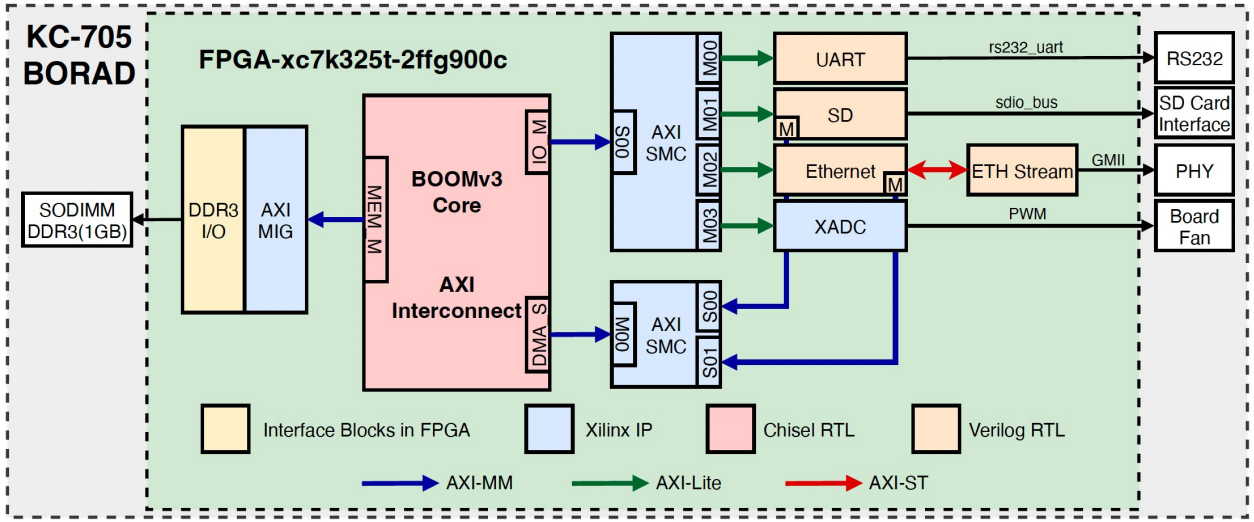
Attackers cannot probe access time differences

Contents

Experimental Setup

- *SpecLFB is implemented in the L1D cache of open-source RISC-V core, SonicBOOM and both cache levels of X86 O3 CPU model in Gem5 simulator.*
- *Hardware prototypes based on **Xilinx EK-KC-705 FPGA** platform burned with three **SonicBOOM cores** and running a Linux-kernel-based operating system **are develeped**.*

Processor	SonicBOOM Configurations	Gem5 Configurations
Baseline	Original SonicBOOM	Original O3 CPU
SSE-RV	SonicBOOM enhanced with SSE-RV	\
STT	\	O3 CPU enhanced with STT
SpecLFB	SonicBOOM enhanced with SpecLFB	O3 CPU enhanced with SpecLFB

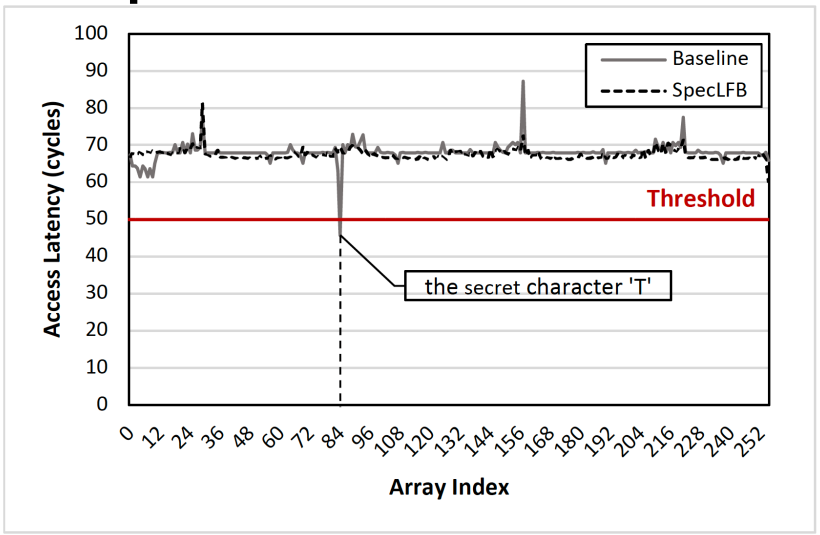


Parameter	SonicBOOM-FPGA	Gem5
ISA	RV64	X86-64
Frequency	FPGA@50MHz	simulate@2GHz
Processor type	2-decode 4-issue MediumBoom O3CPU	8-decode 8-issue DerivO3CPU
ROB/LDQ/STQ	64/16/16 entries	192/32/32 entries
L1I Cache	16KB, 4-way, 64B line	32KB, 8-way, 64B line, 4 MSHRs
L1D Cache	16KB, 4-way, 64B line, 2 MSHRs	32KB, 8-way, 64B line, 4 MSHRs
L2 Cache	512KB, 16-way, 64B line	2MB, 16-way, 64B line, 20 MSHRs

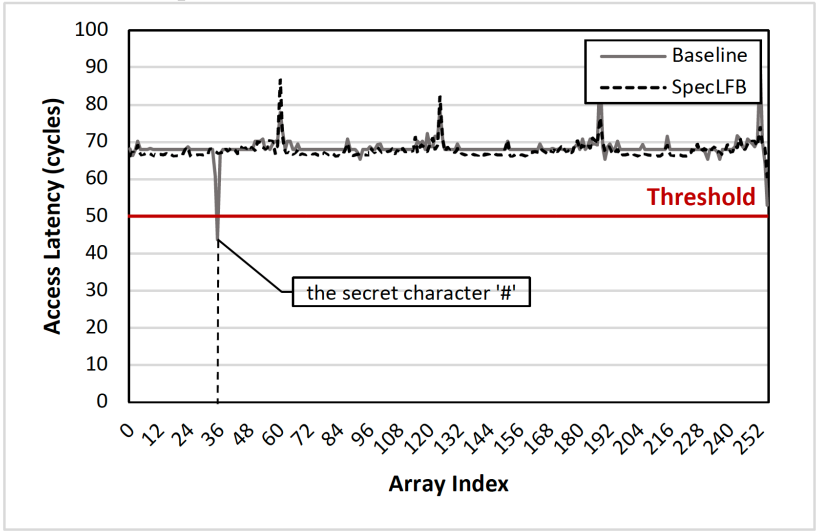
Security Evaluation

- Chipyard-SonicBOOM
- Gem5-X86 O3

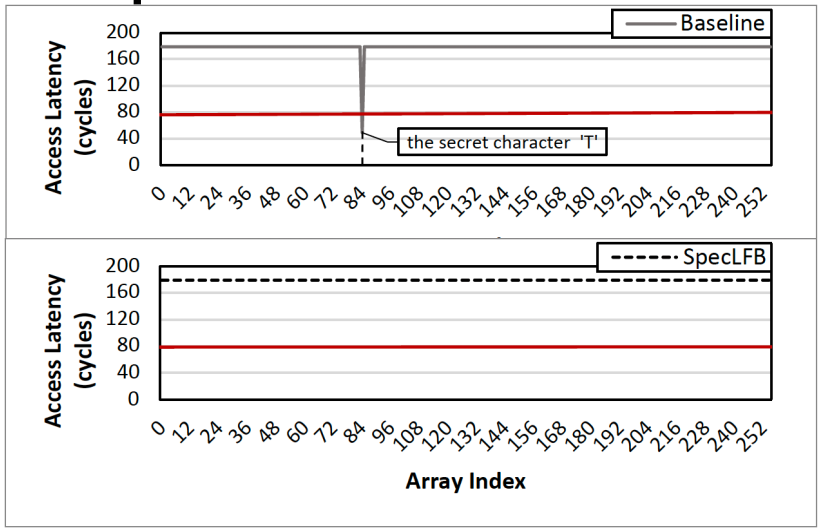
Spectre v1-Evict+Reload



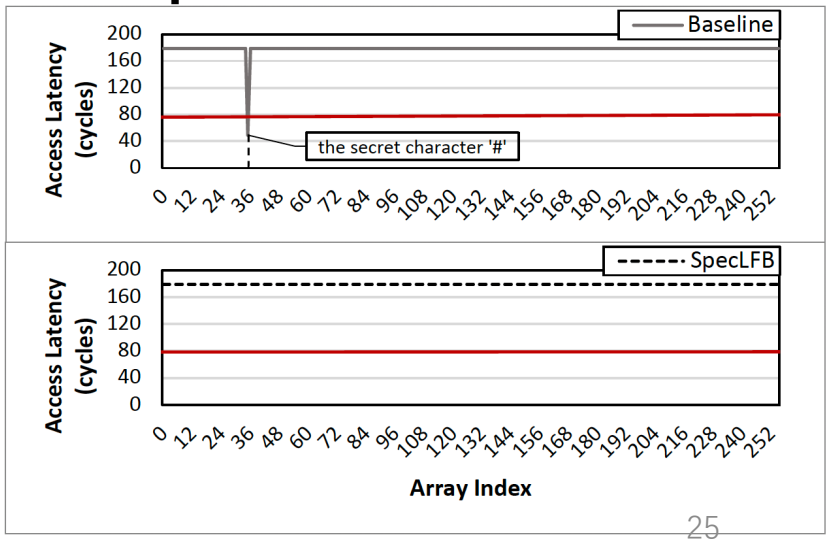
Spectre v4-Evict+reload



Spectre v1-Flush+Reload



Spectre v4-Flush+Reload



Performance Evaluation

Scheme	Performance overhead	Evaluation Method	Speculation			
			Value Prediction	Control Flow	Memory Access	Exception
STT-*Sp*	8.5%	Gem5	✗	✓	✗	✗
STT-*Fu*	14.5%		✓	✓	✓	✓
SpecLFB	3.20%		✗	✓	✓	✓
	1.85%	RTL-FPGA				
SSE-RV	4.8%		✗	✓	✓	✗

- ***Shorter protection time***
- ***Smaller protection scope***
- ***Shorter memory access path after deprotection***

FPGA resources utilization

Scheme	Core	Device	LUTs	FFs
Baseline	SonicBOOM	Xc7a325T	169,463	93,994
SSE-RV	SonicBOOM	Xc7a325T	172,538 (+1.81%)	94,567 (+0.61%)
SpecLFB	SonicBOOM	Xc7a325T	170,765 (+0.77%)	94,283 (+0.31%)

Tips:

LUTs (Look-Up-Tables) *are primarily used to implement logic circuit functionality.*

FFs (Flip-Flops) *are sequential logic elements used for storing and transferring binary data indigital circuits on FPGAs.*

- ***Lower LUT utilization.*** *The additional logic in the taint initialization and propagation stages in SSE-RV is more complex than the security mechanism of SpecLFB.*
- ***Lower FF utilization.*** *SSE-RV adds the taint file, propagation queue, and other intermediate registers related to taint tracking technique, while SpecLFB only adds intermediate registers related to the ROB unsafe mask.*

Contents

Conclusion

- Limit the scope of unsafe speculative loads that need to be delayed to **MUSLs**, which denotes unsafe speculative loads that cause cache misses.
- Introduce a simple yet effective **security check mechanism** that works inconjuction with the **ROB unsafe mask** to the LFB, preventing the cache refill of MUSLs.
- Implemented both in **SonicBOOM** and **Gem5 O3 processor**.
- average hardware resource overhead: **0.6%**

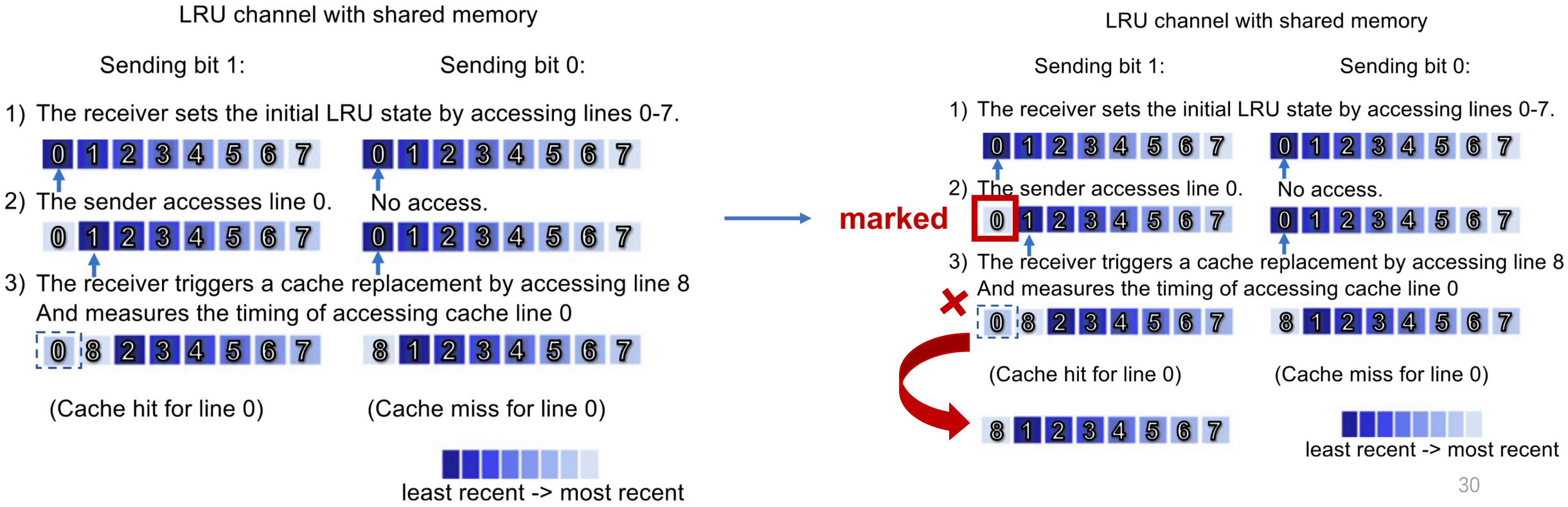
  performance overhead: **1.85% in the FPGA hardware prototype experiment**

  3.20% in the Gem5 simulation

Discussion

Speculative accesses resulting in cache hits. Where a cache replacement (i.e., a cache miss) by the sender is not required to change the cache state.

Example **Speculative Cache side-channel attack based on Least-Recently-Used (LRU) replacement policy [TC' 21]**



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Welcome for questions !

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